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=> d his

     (FILE 'HOME' ENTERED AT 09:29:28 ON 23 JUL 2003)
     FILE 'CA' ENTERED AT 09:29:38 ON 23 JUL 2003
L1    184 S (TRIPLE OR THREE)(1A)(TRACK OR CONDUCTOR)
L2    114 S L1 AND (BIAS OR ELECTRIC?)
L3     10 S L2 AND (NOVEL OR ADVANTAG? OR DISADVANTAG?)
L4     29 S L1(L)(NEW OR DEVELOP?)
L5      2 S L1 AND(SBAR ?/AU OR KOZAKIEWICZ ?/AU)
L6      9 S L2 AND CORRO?
L7     11 S L2 AND TRACK(2A)(TEST? OR DETECT?)
L8      8 S L2 AND PROTECT?
L9   6488 S (TEST? OR EVALUAT? OR EXAMIN? OR MONITOR? OR COMPAR?)(5A)(PROCEDUR?
           OR METHOD? OR PROCESS?)(10A)(PROTECT? OR FAILUR? OR CORRO?)
L10    11 S SBAR ?/AU
L11   313 S L9 AND (IC OR CIRCUIT OR SEMICONDUC?)
L12     7 S L11 AND (TRACK OR INTERDIGI? OR BEAM LEAD? OR COMB)
     FILE 'INSPEC' ENTERED AT 09:59:21 ON 23 JUL 2003
L13    41 S L10
L14    13 S L12
L15     3 S L13 AND(MOISTURE OR ACCELERAT?)AND(COMPAR? OR CIRCUIT)
     FILE 'CA' ENTERED AT 10:10:22 ON 23 JUL 2003
L16    14 S L2 AND FAIL?
L17    64 S L3-8,L12,L16
L18    54 S L17 NOT PY>1999
     FILE 'CA, INSPEC' ENTERED AT 10:15:57 ON 23 JUL 2003
L19    65 DUP REM L18 L14 L15 (5 DUPLICATES REMOVED)

=> d bib,ab 1-65 l19

L19  ANSWER 10 OF 65  CA  COPYRIGHT 2003 ACS on STN
AN   129:48269  CA
TI   Evaluation of die coating materials for chip-on-board technology insertion
     in spaceborne applications
AU   Le, Binh Q.; Nhan, Elbert; Maurer, Richard H.; Lew, Ark L.; Lander, Juan
     R.; Lehtonen, Seppo J.; Darrin, M. Ann Garrison
CS   Applied Physics Laboratory, The Johns Hopkins University, Laurel, MD,
     20723-6099, USA
SO   Proceedings International Conference on Multichip Modules, 6th, Denver,
     Apr. 2-4, 1997 (1997), 142-147 Publisher: Institute of Electrical and
     Electronics Engineers, New York, N. Y.
AB   Chip-on-board (COB) packaging technol. has become increasingly popular for
     miniaturization purposes in high-reliability applications such as
     spaceborne electronics.  It eliminates the hermetic package wt., permits
     the use of conventional soldered devices on an org. substrate (MCM-L), and
     supports rework.  These characteristics provide the much needed
     flexibility to support a faster, better and cheaper electronic design.
     Miniaturization of spaceborne hardware can lead to improvement in
     performance and reliability as well as to cost savings.  The non-hermetic
     nature of COB requires a careful selection of coating materials and a well
     planned process to provide protection against moisture ingress and
     contamination from the surrounding environment.  This paper presents a
     study that evaluates the effects of various die coating materials on bare
     dice and the wire bonding process.  It includes temp. cycling and the
     bias humidity test results on die coating materials as the basis for the
     selection of the most suitable encapsulant material for spaceborne
     applications.
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L19 ANSWER 11 OF 65 CA COPYRIGHT 2003 ACS on STN
AN 129:309221 CA
TI Design dependency of yield loss due to tungsten residues in spin on glass based planarization processes
AU Simon, P. L. C.; Maly, W.; De Vries, D. K.; Bruls, E.
CS Philips Semiconductors Nijmegen, Neth.
SO IEEE International Symposium on Semiconductor Manufacturing, Conference Proceedings, San Francisco, Oct. 6-8, 1997 (1997), P/87-P/90 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
AB In spin on glass (SOG) planarization processes yield loss can occur in between closely spaced metal lines due to the formation of tungsten residues called stringers. Stringers may cause elec. shorts between adjacent metal **tracks**. In this paper it is shown under what conditions stringers may occur, and the extn. procedure capable of detecting locations prone to stringers in a product is proposed. The usefulness of such a procedure for both **failure** anal. and in line **process monitoring** is discussed as well.

L19 ANSWER 14 OF 65 CA COPYRIGHT 2003 ACS on STN
AN 130:102113 CA
TI Sensors for monitoring corrosion in aircraft systems
AU Agarwala, V. S.
CS Aircraft Division, Materials Laboratory, Naval Air Warfare Center, Australia
SO International Corrosion Congress, Proceedings, 13th, Melbourne, Nov., 1996 (1996), Paper 431/1-Paper 431/7 Publisher: Australasian Corrosion Association, Clayton, Australia.
AB A **method** for **monitoring corrosion** in-situ was developed using concepts of dissimilarity (galvanic) in metals which result in an electrochem. change (galvanic current). The galvanic type sensors are **interdigitated** micro strips of two dissimilar metals fabricated on a thin kapton polymer film and galvanically coupled together through a zero resistance **circuit** called ZRA for data acquisition. The noble element in the couple is gold and serves as a cathode while the active metal such as cadmium, zinc, Fe or Ni serves as an anode when short circuited. The output of the sensor showed excellent correlation between the corrosive nature of the environment and the magnitude of the current developed. In particular Au-Cd sensor was most responsive in providing real-time data when used under coatings, lap-joints, BMI-graphite composite lay-ups and in benign (least corrosive) atm. environments. The choice of the active metal is based on the severity of the environment. The sensors were also found suitable when tested in hidden areas of aircraft such as in airframes (fastener and sealant sealed aluminum alloy housings) and on stored aircraft to monitor their exposure conditions or 'health'. The test sites included in this study are: military bases, aircraft carrier flight decks, marine atm. and, operational and stored aircraft and weapon systems. For in-situ corrosivity monitoring sensors were installed in the interior of the aircraft, hidden structures, avionics bays, and embedded under coatings and sealants. The results show a significant correlation between the output of the sensors and the corrosive conditions present. A data base developed from this study may form a basis for condition based maintenance of military hardware in the future.

L19 ANSWER 21 OF 65 CA COPYRIGHT 2003 ACS on STN
AN 123:115420 CA
TI Coupling monolayers for **protection** of microelectronic circuits
AU Fabianowski, Wojciech; Jaccodine, Ralph; Kodnani, Ramesh; Pearson, Raymond; Smektala, Piotr

CS Sherman Fairchild Lab., Lehigh Univ., Bethlehem, PA, 18015-3193, USA
SO Advanced Materials for Optics and Electronics (1995), 5(4), 199-213
AB Two polymeric coatings, a silicone gel (DC 6646) and an epoxy resin (Dexter FP 4402), were glob-top coated onto representative microelectronic circuits, AT&T **Triple Track Testers** (TTTs), and subjected to the pressure cooker test. Coupling monolayers were self- assembled on the TTTs prior to encapsulation to improve the moisture **protection** capabilities of the coatings. Leakage current measurements were made to evaluate the effect of applied monolayers on the moisture **protection** capability. The moisture **protection** capability was assessed in short-term and long-term leakage current measurements. 16-Mercaptohexadecanoic acid and γ-aminopropyltriethoxysilane monolayers, in combination with silicone gel and epoxy resin resp., exhibited very good moisture **protection** performance.

L19 ANSWER 28 OF 65 CA COPYRIGHT 2003 ACS on
AN 118:202930 CA
TI Particle evaluation/control of the titanium/titanium nitride barrier layer in BiCMOS processing
AU Wang, Ping; Liu, Bin; May, Mike; Granum, Mark
CS Motorola, Mesa, AZ, 85202, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (1993), 1802(Microelectronics Manufacturing and Reliability), 69-80
AB Snake/**comb** defect test structures and an in-line patterned wafer inspection system (Inspex) are very effective for monitoring, investigating, and controlling contamination in modern silicon wafer manufg. These techniques have been widely used in our wafer fabrication facility to **monitor** silicon wafer **processing**, and to diagnose device **failures**. Snake/**comb** defect test structures and in-line patterned wafer inspection system were used to evaluate and control Ti/TiN barrier layer particles during silicon wafer processing. The correlation between these two techniques was studied. A defectivity control baseline for Ti/TiN deposition process was established using statistical anal. New and improved preventive maintenance procedures were implemented based on the data from snake and Inspex monitors. As a result, the particle defectivity on the Ti/TiN sputtering process has been dramatically reduced in the Ti/TiN process. The column failures of BiCMOS fast SRAM devices have been reduced by approx. 30%, and the probe yield of the SRAM product line has increased by over 14%.

L19 ANSWER 29 OF 65 CA COPYRIGHT 2003 ACS on STN
AN 119:227386 CA
TI HAST evaluation of organic liquid IC encapsulants using Sandia's assembly test chips
AU Emerson, John A.; Peterson, David W.; Sweet, James N.
CS Sandia Natl. Lab., Albuquerque, NM, 87185, USA
SO Proceedings - Electronic Components & Technology Conference (1992), 42nd, 951-6
AB Highly accelerated stress testing (HAST) expts. were conducted with special-purpose **corrosion** test chips in both bare die form and with various liq. encapsulants: epoxy, silicone and silicone elastomer, or silicone gel. The purpose of the expt. was to show what incremental improvement in die **corrosion** resistance was provided by the encapsulants and to det. the **failure** modes for the two types of samples. The test conditions were 140°, 85% relative humidity, and +40 V **bias** on outer tracks with respect to the center track. In the case of nonencapsulated parts, median lifetimes ≈1000 h for the best passivations were obsd., with the predominate **failure** mode being

triple track corrosion on the die. In the case of the encapsulated parts, the **failure** mode depended on the encapsulant type. Several of the silicone gel materials showed excellent HAST performance, with only a few percent **failures** at the 1100 h point.

L19 ***ANSWER 33 OF 65*** INSPEC (C) 2003 IEE on STN
AN 1991:3999241 INSPEC DN B91068423; C91063751
TI **Failure** coverage of functional **test methods**: a **comparative** experimental **evaluation**.
AU Velazco, R.; Bellon, C.; Martinet, B. (Lab. de Genie Inf., Grenoble, France)
SO Proceedings International Test Conference 1990 (Cat. No.90CH2910-6) Los Alamitos, CA, USA: IEEE Comput. Soc. Press, 1990. p.1012-17 of xvi+1083 pp. 12 refs.
AB An effort has been made to evaluate the fault coverage of functional test methods. A study comparing a structural (manufacturing) test and three functional test methods, a tailored test, a systematic pseudo-exhaustive test, and a random test, is presented. The experiments were performed on defective microprocessors (6800 and 68000). Working with a nonbiased sample of **circuits** was a major concern; thus, randomly distributed defects were created on a set of good **circuits** by cutting either Al or poly-Si **tracks** using microcutter machine equipment. The results concerning defect coverage and Boolean defect coverage are largely better than those given by H.P. Klug (1988). The results indicate that the functional methods evaluated are very thorough. Random test seems to achieve an impressive fault coverage.

L19 ANSWER 36 OF 65 CA COPYRIGHT 2003 ACS on STN
AN 114:33671 CA
TI The effect of volume resistivity on polymer electrical leakage current measurements
AU Troyk, Philip R.; Anderson, James E.
CS Illinois Inst. Technol., Chicago, IL, 60616, USA
SO International SAMPE Electronics Conference (1989), 3(Electron. Mater. Processes), 969-82
AB The authors investigate the theor. prediction of elec. leakage currents for temp.-humidity-bias (THB) tests. An electrostatic finite element model was **developed** for **triple-track** and comb patterns. Using known values for vol. resistivity combined with a specific test pattern geometry, a prediction of leakage currents can be made. The model can be used to compute the leakage current for samples in which polymer-substrate interfacial currents are negligible thus predicting leakage currents for samples which would be expected to pass THB testing.

L19 ANSWER 40 OF 65 CA COPYRIGHT 2003 ACS on STN
AN 110:86436 CA
TI Testing of encapsulants for the protection of electronic components
AU Troyk, Philip R.; Conroy, David; Madigan, Michael
CS Illinois Inst. Technol., Chicago, IL, 60616, USA
SO Polymeric Materials Science and Engineering (1988), 59, 497-501
AB A finite-element model was **developed** for predicting the value of leakage currents for the **triple-track** and comb patterns frequently used to est. failure rates for polymeric integrated circuits. The effects of substrate thickness and resistivity, as well as encapsulant thickness and resistivity could be modeled. The effect of a layer of condensed water on the surface of the encapsulant could also be investigated.

TP 156, C57A5 main

L19 ***ANSWER 43 OF 65*** INSPEC (C) 2003 IEE on STN

AN 1988:3098057 INSPEC DN B88018813
TI Proposed standard environmental test of component coatings.
AU Shanefield, D.J. (Howatt Lab., Rutgers Univ., Piscataway, NJ, USA); Collins, W.R.
SO 1st International SAMPE Electronics Conference. Vol.1. Electronic Materials and Processes
Editor(s): Kordsmeier, N.H., Jr.; Harper, C.A.; Lee, S.M.
Covina, CA, USA: Soc. Adv. Mater. & Process. Eng, 1987. p.70-2 of xiv+750 pp. 6 refs.
AB Committee S-32-1 of the IEEE has been formed to suggest a standard **testing procedure** for coatings used to **protect** electronic components. This procedure is expected to be issued as an IEEE Standard. The procedure involves any of three test devices: thin film resistors, thick film resistors, or a silicon **IC**. Each of these has 'triple **track**' patterns with three parallel conductive lines, folded back and forth many times to cover the surface efficiently. The test device is cleaned, coated with the material to be tested, and placed in an oven at 85 deg. C and 85% relative humidity. An appropriate voltage is imposed between the center conductive line and the outer two grounded lines. Any small electric current ('leakage') is monitored for 1000 hrs, and continuity of the lines is also checked periodically, to detect possible corrosion. A high quality protective coating will provide low leakage currents and no open **circuits**.

L19 ANSWER 53 OF 65 CA COPYRIGHT 2003 ACS on STN
AN 97:48000 CA
TI Improved RTV silicone for IC encapsulant
AU Wong, Ching P.; Maurer, Donald E.
CS Eng. Res. Cent., West. Electr. Co., Princeton, NJ, 08540, USA
SO NBS Special Publication (United States) (1982), 400-72, 275-80
AB The results of BHT (**bias**-humidity-temp.)-TTR (**triple-track** resistor) **testing** showed that the inclusion of crown ethers in a silicone room-temp.-vulcanizable (RTV) formulation dramatically enhances the **elec**. reliability of integrated circuits (IC). These data add further evidence that Na+ and K+ contribute to **failure** of devices, inasmuch as the crowns with the smaller cavities outperform those with larger cavities. The 12-crown-4, with a cavity diam. of 0.18 nm, is most suitable for complexing Na+, with an ion diam. of 0.18 nm. The 15-crown-5, at 0.27 nm, is effective for K+, at 0.26 nm; the 12-crown-4 formulation shows better **elec**. performance than the 15-crown-5 system. The addn. of 15-crown-5 to DCQ3-6550 Gy, the best com. available encapsulant, resulted in a significant improvement in its **elec**. properties.

L19 ANSWER 56 OF 65 CA COPYRIGHT 2003 ACS on STN
AN 91:221191 CA
TI Procurement specification requirements for protection against electromigration failures in aluminum metallizations
AU Sim, S. P.
CS Post Off. Res. Cent., Ipswich, UK
SO Microelectronics and Reliability (1979), 19(3), 207-18
AB Electromigration failure of Al metalization in integrated **circuits** was studied. The sensitivity of electromigration to Al microstructure was confirmed. Temp. and c.d. acceleration factors for the degrdn. of Al **tracks** were found. **Test methods** are recommended which minimize risks of **failure**.

L19 ANSWER 57 OF 65 INSPEC (C) 2003 IEE on STN

AN 1979:1409306 INSPEC DN B79042560
TI New **acceleration** factors for temperature humidity, bias testing.
AU **Sbar, N.L.**; Kozakiewicz, R.P. (Bell Labs. Inc., Allentown, PA, USA)
SO IEEE Transactions on Electron Devices (Jan. 1979) vol.ED-26, no.1, p.56-71. 28 refs.
AB New temperature-humidity **acceleration** factors for surface conductance (G) were determined. These can be used to relate device life in a high-stress laboratory environment to device life in a normal-use environment. Analytical expressions for the **acceleration** factors were derived for both encapsulated and unencapsulated test specimens. Lower **acceleration** factors were predicted for specimens encapsulated with DC 3-6550 RTV silicone rubber than for unencapsulated specimens. The new **acceleration** factors were used to predict failure rates due to electrolytic conduction on active devices.

L19 ***ANSWER 60 OF 65*** INSPEC (C) 2003 IEE on
AN 1978:1142890 INSPEC DN B78005612
TI **Procedures** for **comparative evaluation** of the moisture **protection** of coatings for integrated **circuits**.
AU Kozakiewicz, R.P.; Sbar, N.L. (Bell Telephone Labs. Inc., Allentown, PA, USA)
SO Electrochemical Society Spring Meeting (papers in extended summary form only received)
Princeton, NJ, USA: Electrochem. Soc, 1977. p.123-4 of 1027 pp.
AB Accelerated test procedures involve the use of the triple **track** test **circuit**. This consists of three parallel metallization paths (**tracks**) in a meander pattern on an alumina substrate. The substrate configuration is that of a 24-pin DIP. Each metallization line is approximately 21.6 cm long and 7.6*10-3 cm wide. The space between adjacent lines is also 7.6*10-3 cm. In addition to determining the relative moisture protection afforded by various **circuit** encapsulating materials the test vehicle can be used to evaluate product contamination caused by fabrication processes.

L19 ANSWER 61 OF 65 CA COPYRIGHT 2003 ACS on STN
AN 89:207979 CA
TI Performance of new copper based metallization systems in an 85°C, 80% RH, chlorine contaminated environment
AU **Sbar, N. L.**; Feinstein, L. G.
CS Bell Teleph. Lab., Inc., Allentown, PA, USA
SO Proceedings - Electronic Components Conference (1977), 27, 84-95
AB The performance of Ti-Pd-Cu-Ni-Au and Ti-Cu-Ni + Au metalization systems in an 85°, 80% RH (relative humidity) environment contaminated with Cl was compared with that of the std. Ti-Pd-Au metalization system. Electrolytic and galvanic **corrosion failure** modes were identified for encapsulated (RTV silicone rubber) and unenc0psulated **triple track** samples. Ti-Pd-Cu-Ni-Au and Ti-Cu-Ni + Au metalizations were less resistant to galvanic **corrosion** in the moist Cl contaminated environment than were the Ti-Pd-Au specimens. The RTV silicone rubber encapsulant was extremely effective in retarding galvanic **corrosion** on the 3 metalization systems studied. For the Ti-Cu-Ni + Au and Ti-Pd-Cu-Ni-Au specimens, eventual bond **failures** were the result of penetration of the **corrosive** environment under the edges of the encapsulant.

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STN INTERNATIONAL LOGOFF AT 10:16:55 ON 23 JUL 2003